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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/461,643	12/14/1999	KEITH DOW	10559/108001	4089

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EXAMINER
LEE, CHRISTOPHER E

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 05/09/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/461,643	Applicant(s) DOW, KEITH	
	Examiner Christopher E Lee	Art Unit 2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 December 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

> The oath or declaration is defective because:
> It does not identify the mailing or post office address of each inventor. A mailing or post office address is an address at which an inventor customarily receives his or her mail and may be either a home or business address. The mailing or post office address should include the ZIP Code designation. The mailing or post office address may be provided in an application data sheet or a supplemental oath or declaration. See 37 CFR 1.63(c) and 37 CFR 1.76.

2. Applicant has not given a post office address anywhere in the application papers as required by 37 CFR 1.33(a), which was in effect at the time of filing of the oath or declaration. A statement over applicant's signature providing a complete post office address is required.

Drawings

3. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

4. Figure 1 and Figure 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Note the reference number 115 of Figure 1. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

6. The drawings are objected to because the reference sign 100 of Figure 1 does not delineate a typical computer system from the network 135. The network should not be included in the typical computer system 100 (Fig. 1) Note the description (Page 1, lines 10-18). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

7. The disclosure is objected to because of the following informalities: The Memory Repeater Hub 110 of Figure 1 is referred by a different terminology, Memory Unit 110 (Fig. 1). Note the description (Page 1, lines 10+). The reference signs pin 135 in the description (Page 4, lines 1-4) are not on the Figure 3, but on the Figure 1, which is a Network. The neck down portion 215 (Fig. 4) is not shown as a part of the signal line 200 (Fig. 4). Refer to the description (Page 5, lines 1-2).

Appropriate correction is required.

8. The use of the trademark Rambus has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

Claim Objections

9. Claims 8 and 20 are objected to because of the following informalities: In claim 8, there is an illogical grammatical error on the lines 4-5. In claim 20, the first connection is not on the memory control unit, but on the memory unit (Page 12, lines 7+).

Appropriate correction is required.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 1,2,4-6,9,12-13 and 15-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "the first pin" in line 12. There is insufficient antecedent basis for this limitation in the claim.

Claim 8 recites the limitation "the first pin" in lines 7-8. There is insufficient antecedent basis for this limitation in the claim.

The term "roughly" in claim 2,4-5,9,15-18 is a relative term which renders the claim indefinite. The term "roughly" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The "parallel" means extending in the same direction, everywhere equidistant, and not meeting. The "roughly parallel", however, could be considered as non-parallel. So, it is invalid without a clear definition.

The term "approximately" in claim 5-6,12-13,19 is a relative term which renders the claim indefinite. The term "approximately" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The "equal" means of the same measure, quantity, amount, or number as another. The "approximately equal", however, could be considered as non-equal. So, it is invalid without a clear definition. And, the "5 mils" means the exact 5/1000 inches. The "approximately 5 mils", however, does not clearly specify the range of the value. So, it is invalid without a clear definition.

The term "at least a portion" in claim 2 and 15 is a relative term which renders the claim indefinite. The term "at least a portion" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would

not be reasonably apprised of the scope of the invention. The term "at least a portion" should be clearly defined in the claim in order not to render the claim indefinite.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

13. Claims 1,3,7,8,10,14 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Boaz et al.[USPN 6,061,263]. Since "the first pin" in the claim is not clearly defined. Note above 35 U.S.C. 112 rejection. It is also considered as equivalent to said first connection on said memory unit. In reference to claim 1, Boaz et al. disclose in Figure 1 a computer system comprising: processor (microprocessor 12); memory unit (Rambus memory chip 21) as system memory; memory control unit (memory controller 15) is coupled with said memory unit; and circuit board(motherboard 10 and RIMM PCB-Rambus In-line Memory Module Printed Circuit Board 17) having signal lines between said memory control unit and said memory unit. In addition, Boaz et al. disclose in Figure 1-5 signal lines on said circuit board comprising: a first signal line, formed on a first layer (Fig. 3) of said circuit board (RIMM PCB 17) and connected

between a first connection on said memory unit (Rambus memory chip 21) and said memory control unit (memory controller 15, See Fig. 1-3, col. 2, lines 27-65). A second signal line also formed on said first layer (Fig. 3) of said circuit board (RIMM PCB 17) and connected to said first connection on said memory unit (Rambus memory chip 21), wherein said first layer defines a non-grounded gap between said first and second signal lines (Fig. 3).

In reference to claim 3, Further comprising: third and fourth signal lines, on a second layer of said circuit board (RIMM PCB 17), different than said first layer (Fig. 4).

In reference to claim 7, Said memory unit (Rambus memory chip 21) is a Rambus device.

In reference to claim 8, the method steps of claim 8 are inherently performed by the apparatus of claim 1, and therefore the rejection of claim 1 applies to claim 8.

In reference to claim 10, the method steps of claim 10 are inherently performed by the apparatus of claim 3, and therefore the rejection of claim 3 applies to claim 10.

In reference to claim 14, the method steps of claim 14 are inherently performed by the apparatus of claim 1, and therefore the rejection of claim 1 applies to claim 14.

In reference to claim 16, the method steps of claim 16 are inherently performed by the apparatus of claim 3, and therefore the rejection of claim 3 applies to claim 16.

14. Claim 20 is rejected under 35 U.S.C. 102(e) as being anticipated by Leddige et al.[USPN 6,111,205]. Leddige et al. disclose in Figure 1 a circuit board 100 comprising: memory unit (memory device 110); memory control unit (memory controller 120); data bus (signal traces 130) connecting said memory unit (memory device 110) to said memory control unit (memory controller 120) and comprising: a first signal line (signal traces 130) formed on a selected layer of said circuit board 100 and connected to said memory control unit (memory controller 120) and to a first connection on said memory unit (memory device 110); and a second signal line (signal traces 130) formed on said selected layer of said circuit board and also connected to said first connection on said memory unit (memory device 110).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 2, 9 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boaz et al.[USPN 6,061,263] in view of Kumakura et al.[USPN 6,114,751]. In reference to claim 2, Boaz et al. disclose all the limitations of claim 2 except that do not expressly teach a parallel relationship of said first signal line and a portion of said second signal line. Kumakura et al. disclose a printed circuit board with plural bus channel lines running in parallel with each other (Fig. 25-26). The pitch of said bus channel lines is 0.25mm(10 mils) or 0.375mm(14.75 mils) (See col.19, lines 35+). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have applied the concept of said bus channel lines running in parallel with each other, as disclosed by Kumakura et al., to the signal routing of said first signal line and a portion of said second signal line running in parallel for the advantage of reducing congestion at the memory unit.

In reference to claim 9, the method steps of claim 9 are inherently performed by the apparatus of claim 2, and therefore the rejection of claim 2 applies to claim 9.

In reference to claim 15, the method steps of claim 15 are inherently performed by the apparatus of claim 2, and therefore the rejection of claim 2 applies to claim 15.

17. Claims 4, 11 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boaz et al.[USPN 6,061,263] as applied to claim 2 above, and further in view of Perino et al.[USPN 6,160,716]. In reference to claim 4, Boaz et al. disclose all the limitations of claim 4 except that do not expressly teach that the portion of said second signal line and said first signal line have equal widths. Perino et al. disclose the width of signal trace on a circuit board is determined based

on the impedance to be matched (See col.5, lines 48-49). The claim clearly defines that said signal lines are connected on said memory unit. And, the dielectric thicknesses of said circuit board layer for both of said signal lines are same because both of them are on said first layer. One of ordinary skill in the art would have been motivated to employ the concept of the line width determination, as disclosed by Perino et al., so that the signal line widths of said first and second signal lines are equal because the determined impedance values should be same, for the advantage of eliminating reflected signals and signal deterioration caused by a mismatched impedance (See col. 5 lines 29-32).

In reference to claim 11, the method steps of claim 11 are inherently performed by the apparatus of claim 4, and therefore the rejection of claim 4 applies to claim 11.

In reference to claim 17, the method steps of claim 17 are inherently performed by the apparatus of claim 4, and therefore the rejection of claim 4 applies to claim 17.

18. Claims 5, 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boaz et al.[USPN 6,061,263] as applied to claim 4 above, and further in view of Perino et al.[USPN 6,160,716]. In reference to claim 5, Boaz et al. disclose all the limitations of claim 5 except that do not expressly teach that the portion of said second signal line and said first signal line are separated by a distance equal to said widths of said signal lines. Perino et al. disclose an example, the widths of two traces and the distance between them are equal (See col.5, lines 33-37). Perino et al. teach that the distance spacing is also affecting the value of line impedance (See col.5, lines 37-41). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have set the separating distance equal to said width, for the advantage of eliminating reflected signals and signal deterioration caused by a mismatched impedance (See col. 5 lines 29-32).

In reference to claim 12, the method steps of claim 12 are inherently performed by the apparatus of claim 5, and therefore the rejection of claim 5 applies to claim 12.

In reference to claim 18, the method steps of claim 18 are inherently performed by the apparatus of claim 5, and therefore the rejection of claim 5 applies to claim 18.

19. Claims 6,13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boaz et al.[USPN 6,061,263] as applied to claim 5 above, and further in view of Holman et al.[USPN 6,005,776]. In reference to claim 6, Boaz et al. disclose all the limitations of claim 6 except that said signal lines and said separate distance between them are each 5 mils. Holman et al. teach that PCB technology may include conventional "5/5 routing rules" (See col. 3 lines 60-62) which requires 5 mils spacing between each transmission line and neighboring connection leads. Also, Holman et al. discloses an example which shows 5 mil spacing and 5 mil width of transmission line (See Fig. 4, col.4, lines 15-25). One of ordinary skill in the art would have been motivated to employ the 5 mils line width and spacing, as taught by Holman et al., so that said widths of said lines and said distance separating said lines are set each 5 mils.

In reference to claim 13, the method steps of claim 13 are inherently performed by the apparatus of claim 6, and therefore the rejection of claim 6 applies to claim 13.

In reference to claim 19, the method steps of claim 19 are inherently performed by the apparatus of claim 6, and therefore the rejection of claim 6 applies to claim 19.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Horine [USPN 6,072,699] discloses a signal line routing on a printed circuit board.

Leddige et al. [US 2002/0038405 A1] discloses a method and apparatus for implementing multiple memory buses on a memory module.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter S Wong can be reached on 703-305-3477. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-3718 for regular communications and 703-305-3718 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Christopher E Lee
Examiner
Art Unit 2181

cel/ CEL
May 3, 2002

PETER WONG
SUPERVISORY PATENT EXAMINER
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